**Declararea entitatii (ENTITY)**

Sintaxa:

ENTITY nume\_eticheta IS

GENERIC (lista\_parametrii\_generici);

PORT (lista \_porturi \_I/O);

END nume\_eticheta;

*Exemplu:*

ENTITY sumator IS

GENERIC (latime\_mag: INTEGER:=8);

PORT(a,b: IN std\_logic\_vector (latime\_mag-1 downto 0);

ci: IN std\_logic;

co: OUT std\_logic;

Y: OUT std\_logic\_vector(latime\_mag-1 downto 0 ));

END sumator;

**Declararea arhitecturii (ARCHITECTURE)**

Sintaxa:

ARCHITECTURE nume\_arch OF nume\_ent IS

--Zona declaratii;

BEGIN

--Zona decriere;

END nume\_arch;

*Exemplu:*

ARCHITECTURE dscr exemplu OF exemplu IS

SIGNAL a: IN std\_logic;

BEGIN

WITH sel SELECT

Y<=”0000” WHEN ‘0’,

“0011” WHEN ‘0’,

“1111” WHEN OTHERS;

END dscr\_exemplu;

**Semnalul (SIGNAL)**

Sintaxa:

SIGNAL nume\_semnal{,nume\_semnal}: tip[:valoare\_semnal];

*Exemplu:*

ARCHITECTURE descriere OF mux\_4b IS

SIGNAL a: IN std\_logic;

SIGNAL b: OUT std\_logic:=’0’;

SIGNAL c: BUFFER std\_logic\_vecto r(3 downto 0):=”000”;

BEGIN

--specificații concurente

END descriere;

**Atribuirea concurenta a semnalelor**

Se utilizeaza operatorul “<=”

*Exemplu:*

ARCHITECTURE descr OF ex\_semnal IS

SIGNAL temp: IN std\_logic\_vector(2 downto 0);  
BEGIN

temp<=std\_logic\_vector(a,b);

y<=temp&e;  
END;

**Atribuirea conditionala a semnalelor**

Sintaxa:

nume\_semnal<=<expr> WHEN <conditie>ELSE

<expr.> WHEN <conditie>ELSE

…………………………………………………….

<expr.> WHEN <conditie>ELSE

<expr.>;

*Exemplu:*

Y<= x WHEN en=’0’ ELSE

“zzzzzzz”;(OTHERS=>’z’);

**Atribuirea selectiva a semnalelor**

Sintaxa:

WITH expresie\_selectie SELECT

Nume\_semnal<=<expresie> WHEN <selectie>,

<expresie> WHEN <selectie>,

………………………….

<expresie> WHEN <selectie>,

<expresie> WHEN OTHERS ;

*Exemplu:*

WITH sel SELECT

y<= a WHEN “00”,

b WHEN “10”,

c WHEN OTHERS;

**Declararea unei componente**

Sintaxa:

COMPONENT nume\_componenta IS

PORT(lista porturi);

END COMPONENT;

*Exemplu:*

COMPONENT dec\_7 seg IS

PORT(r:std\_logic\_vector(3 downto 0);

oe:IN std\_logic;

seg:OUT std\_logic\_vector(6 downto 0));

END COMPONENT;

**Instantierea unei componente:**

1. Asociere pozitionala

Sintaxa: Eticheta:nume\_componenta(nume\_semnal1[,nume\_semnal\_n]),

*Exemplu:*

U1:dec\_7seg PORT MAP(t\_data,t\_oe,t\_seg);

1. Asocietea dupa nume

Sintaxa:

Eticheta: nume\_comp PORT MAP (nume\_port1=> nume\_semnal1[, nume\_portn=> nume\_semnaln])

*Exemplu:*

U1 dec\_7seg PORT MAP(data=>t\_data, oe=>t\_oe, seg=t\_sg);

**Specificatia GENERATE**

Sintaxa:

eticheta:IF conditie GENERATE

--Specificatii concurente;

END GENERATE;

*Exemplu:*

IF I<6 GENERATE

--Specificatii concurente;

END GENERATE;

Sintaxa:

eticheta: FOR parametru IN interval GENERATE

--Specificatii concurente;

END GENERATE;

*Exemplu:*

FOR 134 downto 0 GENERATE

U1 sum\_1b PORT MAP(a(k),b(k));

END GENERATE;

**Declararea unui proces**

Sintaxa: eticheta PROCESS(lista senzitivitate)

--Declaratii locale

BEGIN

--Specificatii secventiale;

END PROCESS;

**Declararea unei variabile**

Sinataxa:

VARIABLE :nume variabila[, nume variabila] tip\_variabila[:=valoare\_initiala]

*Exemplu:*

PROCESS(a,b)

VARIABILE c,d

BEGIN

c:=a;

d:=b;

e:=d+a;

END PROCESS;

**Specificatia conditionala “IF/”THEN**

Sintaxa:

IF conditie booleana THEN

--Specificatii secventiale;

ELSE

--Specificatii secventiale;

END IF;

*Exemplu:*

IF cs=’1’ THEN Boot=’1’;

ELSE ROM=’1’;

END IF;

Sintaxa :

IF conditie\_booleana THEN

--Specificatii secventiale

ELSIF conditiie\_booleana THEN

--Specificatii secventiale

……………….....……….

ELSE

--Specificatii\_secventiale;

END IF;

*Exemplu:*

IF(cs>’1’)’ THEN X=’2’;

ELSIF(load=’1’) X=’1’;

ELSE X=’0’;

END IF;

**Specificatia CASE**

Sintaxa:

CASE expresie IS

WHEN sel\_val1=> grup\_specif\_secventiale;

WHEN sel\_val2=> grup\_specif\_secventiale;

……………………………………………………

WHEN sel\_valn=> grup\_specif\_secventiale;

WHEN OTHERS=> grup\_specif\_secventiale;

**Specificatia LOOP**

Sintaxa:

{eticheta} modul iteratie LOOP

--Specificatii secventiale

End LOOP;

1. Model conditional

Sintaxa:

WHILE conditie LOOP

--Grup specificatii secventiale;

END LOOP;

*Exemplu:*

contor=0;

WHILE contor<x”00” LOOP

Contor=contor+’1’;

END LOOP

1. Model iterative

Sintaxa:

FOR valoare\_contor IN interval LOOP

--Grup specificatii secventiale;

END LOOP;

*Exemplu:*

FOR i 0 TO lat\_mag\_1 LOOP

rez(i)<=a(i) XOR b(i) XOR temp(i);

END LOOP;

**Specificatia NEXT**

Sintaxa:

NEXT{nume/eticheta\_bucla}

NEXT{nume/eticheta\_bucla} WHEN conditie;

**Specificatia EXIT**

Sintaxa:

EXIT{eticheta\_bucla}

EXIT{eticheta\_bucla}WHEN conditie;